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7 Multiplexed Wireless Receiver and Transmitter

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9 Field of the Invention

10 This invention relates to an architecture for the  
11 sharing of resources used in the analog front end of a  
12 wireless receiver and transmitter. The resources include  
13 analog to digital converters (ADC) and digital to analog  
14 converters (DAC) commonly used to interface entirely digital  
15 signal processors to entirely analog baseband receivers and  
16 transmit modulators.

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18 Background of the Invention

19 RF amplifiers, mixers, and filters are well known in  
20 the art of high frequency signal processing. An RF  
21 transmitter takes a baseband signal and modulates to a  
22 transmit frequency using an oscillator, mixer, and  
23 amplifiers. Typically, in an RF receiver, an amplifier  
24 increases the signal delivered by an antenna, and it is  
25 mixed to an intermediate frequency, or baseband frequency,

1 and receives additional amplification. Prior art  
2 transmitters and receivers are typically constructed from  
3 high speed transistors and gain elements, and operate as  
4 analog elements, whereby a changing signal level on a single  
5 conductor carries all of the information required in the  
6 signal. For systems carrying analytic signals, a quadrature  
7 pair of signals is sufficient to fully describe the analytic  
8 signal.

9 Figure 1 shows a prior art RF receiver comprising a  
10 baseband receiver 100, analog-digital conversion interface  
11 120, and digital baseband receive processor 136, as well as  
12 a prior art transmitter comprising a digital baseband  
13 transmit processor 230, an analog-digital conversion  
14 interface 232, and a transmit modulator 200 coupled to a  
15 transmit antenna 202. These receiver and transmitter  
16 systems are well known for use in an 802.11 wireless system  
17 for receiving and transmitting ethernet packets. The  
18 baseband receiver 100 is shown as a dual conversion baseband  
19 receiver, and includes a receive antenna 102 for receiving  
20 incoming signals, an optional IF conversion stage 110, which  
21 includes a preamplifier 104 with an RF gain control 280 for  
22 control of preamplifier 104 gain. The preamplifier 104  
23 drives a mixer 106, which also receives an input from a  
24 first local oscillator 108 such that the output of mixer 106  
25 includes an image frequency at an intermediate frequency

1 (IF), which is filtered by IF bandpass filter 238. The IF  
2 amplifier 240 receives this signal from the IF bandpass  
3 filter 238, and increases or decreases the signal level via  
4 IF gain control 242 before passing the signal on to the  
5 quadrature mixers 112 and 116, which are driven by  
6 quadrature oscillators 114 and 118. The quadrature mixing  
7 process generates quadrature outputs comprising an in-phase  
8 (I) and quadrature (Q) signal, which are the quadrature  
9 signal outputs of baseband receiver 100. The IF amplifier  
10 240, or any subsequent stage which does signal processing  
11 after the variable gain control has been performed,  
12 generates a Receive Signal Strength Indicator (RSSI) status  
13 output 244, which is an analog signal related to signal  
14 strength after final amplification. This signal may be used  
15 by the digital baseband receive processor 136 to formulate  
16 the RF gain control 280 and IF gain control 242, which are  
17 analog signals after conversion by digital to analog  
18 converters (DAC) 134 and 132, respectively. Analog-digital  
19 converter interface 120 provides a conversion between the  
20 analog signal processing functions found in the baseband  
21 receiver 100 and the digital baseband receive processor 136.  
22 Analog quadrature baseband signals from the quadrature  
23 mixers 112 and 116 are filtered by low pass filters 124 and  
24 128 before being digitized by analog to digital converters  
25 (ADC) 126 and 130, respectively. The analog-digital

1 converter interface 120 also converts the analog RSSI status  
2 signal 244 into digital output for the digital baseband  
3 receive processor 136 status input, which also generates  
4 digital control outputs for IF gain and RF gain, which are  
5 fed to digital to analog converters (DAC) 132 and 134,  
6 respectively. The digital baseband receive processor 136 is  
7 generally an entirely digital functional block, which  
8 receives digital values and generates digital values, and  
9 these values are converted to and from analog values by the  
10 analog-digital converter interface 120, as has been  
11 described. In addition to RF and IF gain control management  
12 in response to either the RSSI status input or actual  
13 values presented to the in-phase (I) and quadrature (Q)  
14 channel interfaces, typical functions performed by the  
15 digital baseband receive processor 136 include signal stream  
16 synchronization, symbol extraction, demodulation, packet  
17 framing, and packet buffer management of ethernet packets  
18 received across analog-digital converter interface 120.

19 In addition to the double conversion heterodyne  
20 receiver shown in baseband receiver 100 which includes IF  
21 conversion stage 110, it is possible to omit the IF  
22 conversion stage 110 to form a direct, or single conversion  
23 receiver. In this case, incoming signals from receive  
24 antenna 102 are applied directly to IF amplifier 240, which  
25 is now acting as a gain controlled RF amplifier, in place of

1 preamplifier 104. The output of the gain controlled RF  
2 amplifier 240 is fed to quadrature mixers 112 and 116.  
3 These quadrature mixers 112 and 116 are also receiving  
4 signals from quadrature oscillators 114 and 118 at the  
5 incoming RF frequency, thereby achieving direct baseband  
6 conversion and delivering quadrature outputs to analog-  
7 digital converter interface 120, as before.

8       The digital baseband transmit processor 230 of figure  
9 1 performs analogous operations for the transmission of  
10 signals. Digital baseband transmit processor 230 removes  
11 packets for transmission from a packet buffer which may be  
12 shared with digital baseband receive processor 136, and  
13 converts the packet into a modulated baseband stream of  
14 quadrature digital data, which is digitized by digital to  
15 analog converters (DAC) 218 and 220, and then filtered by  
16 low pass filters 222 and 224. The resulting quadrature data  
17 stream from low pass filters 222 and 224 is converted to a  
18 modulation frequency by mixers 210 and 214 which are both  
19 fed by transmit oscillator 212. The signals are summed 206  
20 and a single modulation product at the desired range of  
21 frequencies is selected via bandpass filter 208 and fed to  
22 power amplifier 204 which drives the transmit antenna 202.  
23 The power amplifier 204 accepts a gain control input 234,  
24 and also produces an RF output level status 236. The RF  
25 output level status 236 is converted by an ADC 228 and read

1 by the digital baseband transmit processor 230, which may  
2 respond with a different value of digital transmit (TX)  
3 gain, which is converted by DAC 226 to TX gain control input  
4 234 and fed to RF power amplifier 204. As with the digital  
5 baseband receive processor 136, the digital baseband  
6 transmit processor 230 is a function implemented using  
7 entirely digital components which may be integrated into a  
8 single digital integrated circuit or field programmable gate  
9 array (FPGA).

10 The digital signal processing of figure 1 is well known  
11 to one skilled in the art, and may be found in the  
12 disclosure of other wireless systems such as that described  
13 in U.S. Patent No. 6,563,858 by Fakatselis et al, or in the  
14 datasheet for Intersil ISL3873B, datasheet number FN8019.2.

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16 Objects of the Invention

17 A first object of the invention is an apparatus for  
18 sharing functional blocks of a receive processor and a  
19 transmit processor with a baseband receiver and a modulator.

20 A second object of the invention is an apparatus for  
21 sharing digital to analog converters (DAC) between a receive  
22 processor and a transmit processor.

23 A third object of the invention is an apparatus for  
24 sharing analog to digital converters (ADC) between a receive  
25 processor and a transmit processor.

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2 Summary of the Invention

3       A digital transmit processor generates quadrature  
4 transmit data during a transmit time, and a digital receive  
5 processor generates a plurality of gain control signals  
6 during a receive time. A multiplexer selects between  
7 quadrature transmit data and receive gain control signals  
8 and furnishes these to a multiplexer which delivers the  
9 selected values simultaneously to a baseband processor  
10 requiring said plurality of gain control signals and a  
11 transmit modulator requiring said plurality of quadrature  
12 transmit data. The baseband receiver generates a received  
13 signal strength indicator (RSSI) as an analog signal and the  
14 transmit modulator generates a transmit power indicator as  
15 an analog signal, and these are selected by an analog  
16 switch, digitized, and fed to the baseband receive processor  
17 and the baseband transmit processor. Unless the baseband  
18 transmit processor is transmitting, the multiplexers of the  
19 invention are selecting receive baseband processor signals,  
20 and when the transmitter is enabled, the multiplexers are  
21 selecting transmit processor signals.

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1    Brief Description of the Drawings

2            Figure 1 shows the block diagram for a prior art  
3 receiver and transmitter.

4            Figure 2 shows the block diagram for a receiver and  
5 transmitter including multiplexed digital-analog converters.

6            Figure 3 is the block diagram for a receiver and  
7 transmitter including multiplexed digital-analog converters.

8            Figure 4 shows a timing diagram for the operation of  
9 the receiver-transmitter of figure 3.

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12    Detailed Description of the Invention

13            Figure 2 shows the baseband receiver 100, and transmit  
14 modulator 200 of figure 1, having inputs and outputs as were  
15 described earlier. The baseband receiver generates a pair  
16 of quadrature analog output signals 360 and 362, as well as  
17 a received signal strength indicator (RSSI) 244, and accepts  
18 as inputs analog signals RF gain control 280 and IF gain  
19 control 242. As was described for figure 1, block IF  
20 conversion stage 110 including RF gain control 280 of figure  
21 2 is only present for a heterodyne receiver with an IF  
22 conversion stage 110, and for a direct conversion receiver,  
23 IF conversion stage 110 is not present. The transmit  
24 modulator 200 of figure 2 has quadrature digital inputs 364



1 and 366, Tx gain control 234, and generates transmit power  
2 RF output level status 236.

3 During non-transmit intervals, inactive transmit enable  
4 signal 386 is 0, which causes multiplexers 384, 396, and 398  
5 to select the "0" input, whereby the RSSI status input 244  
6 is fed to ADC 388, and is applied to RSSI status input of  
7 digital baseband receive processor 330. The IF and RF gain  
8 control outputs of the digital baseband receive processor  
9 330 are applied to multiplexers 396 and 398, respectively,  
10 which select the "0" inputs of multiplexers 396 and 398  
11 associated with inactive transmit enable signal 386, and the  
12 IF and RF gain control signals are generated by DAC 380 and  
13 382, respectively, and fed to the baseband receiver 100.  
14 These signals are also delivered to the transmit modulator  
15 quadrature inputs 364 and 366, but have no effect, as the  
16 transmit enable signal 386 is also provided to the transmit  
17 modulator 200 and may be delivered to any point which causes  
18 the transmitter to be disabled, such as power amplifier 204  
19 control signal Tx Enable.

20 During transmit intervals, the transmit enable signal  
21 386 is active, or "1", which causes multiplexers 384, 396,  
22 and 398 to select the "1" input. In this mode, the  
23 quadrature outputs 368 and 370 of the digital baseband  
24 transmit processor 394 drive multiplexers 396 and 398,  
25 respectively, providing input to DACs 380 and 382, thereby

1 providing the quadrature inputs 364 and 366, respectively,  
2 to transmit modulator 200. The transmitter is enabled by  
3 the transmit enable signal 386, when enables the power  
4 amplifier 204 to send the resulting mixed, up-converted, and  
5 amplified signals to the transmit antenna 202. The  
6 transmitted output power indication RF output level status  
7 236 is passed to multiplexer 384, which has special  
8 provision to pass analog signals to ADC 388, which sends  
9 the Tx power level to the power detector input of the  
10 digital baseband transmit processor 394 as well as the RSSI  
11 input, which is ignored when transmit enable signal 386 is  
12 active. The digital baseband receive processor 330 ignores  
13 the signals presented to it during the transmit interval as  
14 identified by the transmit enable signal 386, using any  
15 mechanism known in the art of transmitter-receivers also  
16 known as transceivers. An analogous problem for the prior  
17 art receiver of figure 1 is the handling of signals found on  
18 quadrature inputs of digital baseband receive processor 136  
19 during transmit intervals while the digital baseband  
20 transmit processor 230 is sending signals which are  
21 amplified to transmit antenna 202 which couple into receive  
22 antenna 102 and decode to quadrature inputs of digital  
23 baseband receive processor 136. This problem is often  
24 solved by having the digital inputs of the digital baseband  
25 receive processor 136 qualified by a signal such as a

1 transmit enable signal which is generated by digital  
2 baseband transmit processor 230.

3 In this manner, the transmit enable signal 386 of  
4 figure 2 controls multiplexers 384, 396, 398, which select  
5 either receiver-related inputs or transmit-related inputs.  
6 The transmit enable signal 386 is only asserted true upon  
7 transmit, and at other times, the system is receiving  
8 packets. During transmit intervals, the proper transmit  
9 signals are routed to the transmit processor, and during  
10 receive intervals, the proper receive signals are routed to  
11 the receive processor. In this manner, the receiver and  
12 transmitter functions operate properly and independently.

13 Figure 3 shows a more efficient embodiment of the  
14 multiplexed receiver transmitter of figure 2 including  
15 modified baseband receive processor 410 and modified  
16 baseband transmit processor 412. Figure 2 used three DAC  
17 elements (378, 380, 382) and three ADC elements (326, 328,  
18 388). Additional multiplexing of converters in figure 3  
19 reduces this to two ADCs (326, 328) and two DACs (380, 382).  
20 In figure 3, the transmit enable signal 386 controls an  
21 additional multiplexer 402, and an additional multiplexer  
22 400 changes state during the receive interval under control  
23 by RSSI mux control signal 408 from baseband receive  
24 processor 410. During the initial part of the packet  
25 receive, RSSI mux control signal 408 selects the RSSI signal

1 244 until a packet is being received, whereafter the RSSI  
2 measurement is taken and the RSSI mux control signal 408  
3 switches to select the I channel 360 after filter 320. The  
4 Q channel 362 is selected by transmit enable signal 386 and  
5 delivered to ADC 328. The output of ADC 328 is delivered to  
6 both the baseband transmit processor 412 power detector  
7 status input, and to the Q channel of baseband receive  
8 processor 410. Multiplexer 402 is selecting the filtered  
9 quadrature receive Q channel 362 when transmit enable signal  
10 386 is not active, and is selecting the tx power 236 when  
11 transmit enable signal 386 is active. The output of ADC 326  
12 is delivered to both the I channel of the baseband receive  
13 processor 410 and the RSSI input of the baseband receive  
14 processor 410. The Tx gain control input 234 of the  
15 transmit modulator 200 is generated by the output of an  
16 analog sample and hold 404, which follows the analog input  
17 generated by DAC 380 when sample control 406 is asserted,  
18 and holds the last value sampled when sample control 406 is  
19 not asserted. In this manner, the Tx gain may be encoded  
20 into the I channel 368, selected during transmit time by  
21 multiplexer 396, converted into an analog signal by DAC 380,  
22 sampled with a value held by sample control 406, and this  
23 value held and presented as the Tx gain control input 234.

24 Figure 3 also includes an optional test mode, whereby  
25 the first DAC 380 generates an analog output A 420 which is

1 coupled to a test input t of multiplexer 400 and second DAC  
2 382 generates an analog output B 422 which is coupled to  
3 multiplexer 402 test input t. In this manner, it is  
4 possible to add test functionality whereby the ADC  
5 multiplexers 400 and 402 are configured to select a test  
6 input A 420 and B 422, which are the values generated by DAC  
7 380 and 382, respectively, in response to IF Gain and RF  
8 gain from bandpass receive processor 410, or in response to  
9 I and Q channel outputs 380 and 370 of baseband transmit  
10 processor 412. These represent optional outputs and  
11 inputs which may be used for end-to-end testing the  
12 functionality of the converter interface 324 through both  
13 DAC and ADC converters. It should also be clear to one  
14 skilled in the art that the digital outputs of the baseband  
15 receive processor 410 and baseband transmit processor 412  
16 are two or more bits wide as known to one skilled in the art  
17 of digital representations of analog signals, and the  
18 multiplexers 400 and 402 perform as analog switches, in that  
19 their inputs and outputs are analog waveforms which are  
20 passed from input to output with minimal change in the  
21 voltage being passed, controlled by a digital select value  
22 which selects which input is to be passed to the output.  
23 This is in contrast to the multiplexers 396 and 398 which  
24 are passing a plurality of digital signals representing the  
25 two or more bit wide digital representations of these

1 signals prior to conversion to analog signals by DACs 380  
2 and 382. The test inputs of multiplexers 400 and 402 may be  
3 connected to either DAC output 380 or 382, and the same end-  
4 to-end test mechanism may be provided on the system of  
5 figure 2 by allowing the multiplexer 384 to accept an output  
6 from one or more of DAC 378, 380, or 382.

7 Figure 4 shows the timing diagram for figure 3 during a  
8 receive event and a transmit event. Transmit enable signal  
9 386 divides the timing diagram into a receive interval 516  
10 and a transmit interval 518. When transmit enable signal  
11 386 is not asserted, receive interval 516 is shown with  
12 incoming packet 500, which includes a preamble and data.  
13 The baseband receiver outputs 360 and 362 carry the  
14 quadrature preamble shown as pre-I and pre-Q followed by  
15 packet data shown as data-I and data-Q. During the preamble  
16 time, the receive processor 410 determines the signal  
17 strength and achieves codeword synchronization, and during  
18 the data interval, the receive processor 410 demodulates the  
19 data stream. During the entire packet, RSSI signal 244  
20 indicates the receive power level, the baseband receive  
21 processor 410 notes this level, and uses it to make any  
22 necessary change to the levels of IF gain control 502 or RF  
23 gain control 504, which are selected by multiplexers 396 and  
24 398, respectively, converted to analog signals, and  
25 delivered to the receiver during receive interval 516 as IF

1 gain 242 and RF gain 280, respectively. The presence of a  
2 packet as determined by the baseband receive processor 410  
3 RSSI input also causes RSSI mux control signal 408 to  
4 assert, thereby causing the I channel 508 to switch from  
5 RSSI to preamble and data, as shown. The Q channel 508  
6 continues to carry preamble-Q and data-Q during the receive  
7 interval 516, as shown.

8       During the transmit interval 518, the baseband receive  
9 processor 410 ignores the tx power level which is now  
10 multiplexed into Q channel input, while the power detect  
11 input 514 of the baseband transmit processor 412 uses this  
12 information to control the transmit gain by sending this on  
13 the I channel 368 and asserting sample control 406. This  
14 causes the sample and hold 404 of figure 3 to retain this  
15 value and send it as transmit modulator input Tx gain  
16 control input 234, as shown on figure 4. The transmit gain  
17 information 520 is placed into the I channel 368 before the  
18 preamble begins, so that the I channel 368 and Q channel 370  
19 present valid quadrature data for modulation by transmit  
20 modulator 200 during transmit interval 518. Tx power 236 is  
21 also delivered to the transmit modulator using transmit  
22 modulator inputs 364 and 366, which results in RF output 512  
23 to be radiated from the transmit antenna 202.

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